In the Specification:

Please replace the following paragraphs with the changes shown in marked-up form:

On p. 8, paragraph 31:

In one mode of operation, the data-in register 395 of the controller 110 receives a data strobe from the input buffer 397 and data from the input buffer 399. The input buffer 397 is enabled by the read indicator 396 and the input buffer 399 is enabled by the read indicator 398. The input buffer 397 receives input (i.e., a data strobe) from the DS lead 170 and the input buffer 399 receives input (i.e., data) from the DQ lead 160. The control logic 580 in controller 110 sets the read indicators 396, 398 to enable the input buffers 397, 399 when receiving data from a DRAM 130. The received data strobe, therefore, clocks the receipt of the data.

On p. 11, paragraph 40:

Figure 3 illustrates a DRAM 130 of the memory system 100. As illustrated in Figure 3, the DRAM 130 includes a mode register 302, C/A register 310, a transmit (Tx) indicator 320, an output buffer 325, a receive (Rx) indicator 330, an input buffer 335, a data-in register 340, a receive indicator 350, an input buffer 355, a transmit (Tx) indicator 360, an output buffer 365, a data-out register 370 and an AND gate 305 ~~304~~. In some embodiments, the two receive indicators 330 and 350 are the same receive control signal, and the two transmit indicators 320 and 360 are the same transmit control signal. Furthermore, the receive and transmit indicators may be complements of each other.

On p. 12, paragraph 44:

The DRAM mode register 302 stores a directional mode when used in conjunction with the DRAM 130 (or the DRAM 440 of Figure 4). The directional mode determines whether the DS leads 170 are unidirectional or bidirectional. The mode register 302 may preferably be set during operation of the DRAM 130 by the controller 110 or during the manufacture of the DRAM 130 or memory module 120. In some embodiments, the controller 110 and DRAM 130 are configured so that the controller may send a command

over the control and address lines 150 that directs the DRAM to store a particular mode value in the mode register 302. The directional mode stored by the mode register 302 is transmitted to the AND gate 305 ~~304~~.

On p. 12, paragraph 45:

The AND gate 305 ~~304~~, as indicated in the preceding paragraph, receives input from the DRAM mode register 302. The AND gate 305 ~~304~~ also receives input from the transmit (Tx) indicator 320. The output of the AND gate 305 ~~304~~ is high if the directional mode is high and the transmit (Tx) indicator 320 is high. Preferably, the transmit (Tx) indicator 320 and the directional mode are high when the DRAM 130 transmits a data strobe to the controller and the DRAM 130 is configured to operate in a bidirectional mode. The output of the AND gate 305 ~~304~~ is connected to the output buffer 325 to enable or disable the output buffer 325. So when the DRAM 130 transmits data and, in addition, the DRAM 130 is configured to operate in a bidirectional mode, the output buffer 325 is enabled and drives the received clock signal onto the DS lead 170 as the data strobe for the data being transmitted from the data out register 370. Conversely, when the DRAM 130 is configured to operate in a unidirectional mode, the output of the AND gate 305 ~~304~~ is low such that the output buffer 325 is disabled. When the output buffer 325 is not enabled, its output is tristated (i.e., set to a high impedance state), which leaves the DS lead 170 floating if no other device is asserting a signal on the DS lead, and more generally allows the DS lead 170 to be driven by another device (e.g., the memory controller 110, or another memory device in another memory module on the same memory bus as the memory module 120 in which the DRAM 130 resides).

On p. 14, paragraph 54:

Figure 5B illustrates another embodiment of a DRAM 450 for use in the memory system 100. Unlike the DRAMs 130, 440 of Figures 3 and 4, this DRAM 450 does not include an AND gate 305 ~~304~~ or an output buffer 325. This is because this DRAM 450 does not transmit a data strobe over the DS lead 170. Additionally, this DRAM 450 does not include a multiplexor 410 because the output of the data-out register 370 is not clocked or timed by the clock. Instead, the data-out register 370, like the data-in register 340, is always

clocked by a data strobe transmitted over the DS lead 170. Preferably, only control and address signals transmitted over the C/A lead 150 are clocked by the clock. This DRAM 450 is compatible with controllers described herein (e.g., controller 110 and controller 425), but is not compatible with conventional controllers.